This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Original) A method for fabricating a transistor in a semiconductor device, the method comprising:

(a) sequentially depositing a buffer insulation layer and a first insulation layer on a semiconductor substrate;

(b) etching the first insulation layer and the buffer insulation layer and forming poly electrodes for a lightly doped drain (LDD) on sidewalls of the etched portion thereof;

(c) forming a local channel region into the semiconductor substrate under the poly electrodes by performing an local channel ion implantation process;

(d) forming a gate insulation layer on surfaces of the poly electrodes and the semiconductor substrate above the local channel region;

(e) forming a gate electrode by depositing a gate electrode material on the gate insulation layer; and

(f) forming a source and drain region.

2. (Original) A method as defined by claim 1, further comprising forming a gate plug, a source contact plug, and a drain contact plug.

3. (Original) A method as defined by claim 2, further comprising:

forming contact holes through which the gate electrode, the source electrode and the drain electrode are exposed by etching the third insulation layer, the second insulation layer and the buffer insulation layer; and

forming plugs by sequentially depositing and planarizing a conductive material on the resultant structure.

4. (Original) A method as defined by claim 1, wherein, in (b), the buffer insulation layer is not entirely removed and, in (d), the gate insulation layer is formed after removing the buffer insulation layer remaining on the semiconductor substrate.

5. (Original) A method as defined by claim 1, wherein a length of the gate electrode is controlled by the poly electrodes.

6. (Original) A method as defined by claim 1, wherein, in (b), a polysilicon is deposited on sidewalls of the first insulation layer by an in-situ doping process to form the poly electrodes.

7. (Original) A method as defined by claim 1, wherein lateral diffusions of the source electrode and the drain electrode are prevented by the local channel region.

8. (Original) A method as defined by claim 1, wherein, in (e), the gate electrode is formed by performing a blanket etchback process after the gate electrode material is deposited on the gate insulation layer.

9. (Original) A method as defined by claim 1, wherein, in (e), the gate electrode is formed by performing a planarizing process after the gate electrode material is deposited on the gate insulation layer.

10. (Original) A method as defined by claim 9, wherein the planarizing process is a CMP (Chemical Mechanical Polishing) process.

11. (Original) A method as defined by claim 1, wherein, in (f), a silicide is formed on outside surfaces of the gate electrode and the poly electrode by performing a salicidation process before the source electrode and the drain electrode are formed into the semiconductor substrate.

12. (Original) A method as defined by claim 1, wherein, in (f), the source electrode and the drain electrode are formed by performing an impurity ion implantation process.

13. (Original) A method as defined by claim 1, wherein, in (f), the source electrode and the drain electrode are formed by performing a selective epitaxial silicon growth.

14. (Original) A method as defined by claim 1, wherein, in (f), the source electrode and the drain electrode are formed by performing an in-situ doping process of polysilicon.

15. (Original) A method as defined by claim 1, wherein, in (f), the source electrode and the drain electrode are formed by performing an annealing process after depositing boro-silicate glass (BSG) or phospho-silicate glass (PSG).

16. Cancelled

17. Cancelled

18. Cancelled

19. Cancelled